CLAIMS

1. (Currently Amended) A power semiconductor device, comprising:

a base layer of a first conductivity type;

a base layer of a second conductivity type selectively formed on one surface of said base layer of the first conductivity type;

an emitter layer of the first conductivity type selectively formed on the surface of said base layer of the second conductivity type;

a collector layer selectively formed on one of the one surface and another surface of said base layer of the first conductivity type;

a first main electrode formed on said collector layer;

a second main electrode formed on said emitter layer and on said base layer of the second conductivity type;

a gate insulating film formed on and directly contacting a surface of said base layer of the second conductivity type that lies between said emitter layer and said base layer of the first conductivity type, said gate insulating film including a first insulating portion and a second insulating portion; and

a gate electrode formed above said first and second insulating portions,

wherein a capacitance of a capacitor formed of the second insulating portion is smaller than a capacitance of a capacitor formed of the first insulating portion.

2. (Previously Presented) The power semiconductor device according to claim 1, wherein the first insulating portion is formed in a portion near said emitter layer, and the second insulating portion is formed in a portion near said base layer of the first conductivity type.

3. (Previously Presented) The power semiconductor device according to claim 2, wherein a thickness of the second insulating portion is larger than a thickness of the first insulating portion.

4. (Previously Presented) The power semiconductor device according to claim 2, wherein a dielectric constant of the second insulating portion is smaller than a dielectric constant of the first insulating portion.

5. (Previously Presented) The power semiconductor device according to claim 2, wherein a thickness of the second insulating portion has an inclination and the thickness thereof on a side of said emitter layer is smaller than a thickness on a side of said base layer of the first conductivity type.

6. (Previously Presented) The power semiconductor device according to claim 1, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

7. (Previously Presented) The power semiconductor device according to claim 2, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

8. (Previously Presented) The power semiconductor device according to claim 3, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

9. (Previously Presented) The power semiconductor device according to claim 4, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

10. (Previously Presented) The power semiconductor device according to claim 5, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

11. (Currently Amended) A method of manufacturing a power semiconductor device, comprising:

forming a base layer of a first conductivity type;

selectively forming a base layer of a second conductivity type on one surface of the base layer of the first conductivity type;

selectively forming an emitter layer of the first conductivity type on a surface of the base layer of the second conductivity type;

selectively forming a collector layer on one of the one surface and another surface of the base layer of the first conductivity type;

forming a first main electrode on said collector layer;

forming a second main electrode on said emitter layer and on the base layer of the second conductivity type;

forming a gate insulating film on a surface of and in direct contact with the base layer of the second conductivity type that lies between said emitter layer and the base layer of the first conductivity type, said gate insulating film including a first insulating portion and a second insulating portion; and

forming a gate electrode above said first and second insulating portions,

wherein a capacitance of a capacitor formed of the second insulating portion is smaller than a capacitance of a capacitor formed of the first insulating portion.

12. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 11, wherein the first insulating portion is formed in a portion near said emitter layer and the second insulating portion is formed in a portion near said base layer of the first conductivity type.

13. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 12, wherein a thickness of the second insulating portion is larger than a thickness of the first insulating portion.

14. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 12, wherein a dielectric constant of the second insulating portion is smaller than a dielectric constant of the first insulating portion.

15. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 12, wherein a thickness of the second insulating portion has an inclination and the thickness thereof on a side of said emitter layer is smaller than a thickness on a side of said base layer of the first conductivity type.

16. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 11, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

17. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 12, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

18. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 13, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

19. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 14, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

20. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 15, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

21. (Currently Amended) A power semiconductor device, comprising:

a base layer of a first conductivity type;

a base layer of a second conductivity type selectively formed on one surface of said base layer of the first conductivity type;

a source layer of the first conductivity type selectively formed on the surface of said base layer of the second conductivity type;

a drain layer selectively formed on one of the one surface and another surface of said base layer of the first conductivity type;

a first main electrode formed on said drain layer;

a second main electrode formed on said source layer and on said base layer of the second conductivity type;

a gate insulating film formed on and directly contacting a surface of said base layer of the second conductivity type that lies between said source layer and said base layer of the

first conductivity type, said gate insulating film including a first insulating portion and a second insulating portion; and

a gate electrode formed above said first and second insulating portions,

wherein a capacitance of a capacitor formed of the second insulating portion is smaller than a capacitance of a capacitor formed of the first insulating portion.

22. (Previously Presented) The power semiconductor device according to claim 21, wherein the first insulating portion is formed in a portion near said one of said source layer, and the second insulating portion is formed in a portion near said base layer of the first conductivity type.

23. (Previously Presented) The power semiconductor device according to claim 22, wherein a thickness of the second insulating portion is larger than a thickness of the first gate insulating film.

24. (Previously Presented) The power semiconductor device according to claim 22, wherein a dielectric constant of the second insulating portion is smaller than a dielectric constant of the first gate insulating film.

25. (Previously Presented) The power semiconductor device according to claim 22, wherein a thickness of the second insulating portion has an inclination and the thickness thereof on a side of said source layer is smaller than a thickness on a side of said base layer of the first conductivity type.

26. (Previously Presented) The power semiconductor device according to claim 21, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

27. (Previously Presented) The power semiconductor device according to claim 22, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

28. (Previously Presented) The power semiconductor device according to claim 23, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

29. (Previously Presented) The power semiconductor device according to claim 24, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

30. (Previously Presented) The power semiconductor device according to claim 25, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

31. (Currently Amended) A method of manufacturing a power semiconductor device, comprising:

forming a base layer of a first conductivity type;

selectively forming a base layer of a second conductivity type on one surface of the base layer of the first conductivity type;

selectively forming a source layer of the first conductivity type on a surface of the base layer of the second conductivity type;

selectively forming a drain layer on one of the one surface and another surface of the base layer of the first conductivity type;

forming a first main electrode on the drain layer;

forming a second main electrode on the source layer of the first conductivity type and on the base layer of the second conductivity type;

forming a gate insulating film on and in direct contact with a surface of the base layer of the second conductivity type that lies between the source layer of the first conductivity type and the base layer of the first conductivity type, said gate insulating film including a first insulating portion and a second insulating portion; and

forming a gate electrode above said first and second insulating portions,

wherein a capacitance of a capacitor formed of the second insulating portion is smaller than a capacitance of a capacitor formed of the first insulating portion.

32. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 31, wherein the first insulating portion is formed in a portion near said source layer and the second insulating portion is formed in a portion near said base layer of the first conductivity type.

33. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 32, wherein a thickness of the second insulating portion is larger than a thickness of the first insulating portion.

34. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 32, wherein a dielectric constant of the second insulating portion is smaller than a dielectric constant of the first gate insulating film.

35. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 32, wherein a thickness of the second insulating portion has an inclination and the thickness thereof on a side of said source layer is smaller than a thickness on a side of said base layer of the first conductivity type.

36. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 31, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

37. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 32, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

38. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 33, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

39. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 34, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

40. (Previously Presented) The method of manufacturing a power semiconductor device according to claim 35, wherein said gate electrode is buried in a trench with the first and second insulating portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.